

CLAIMS

What is claimed is.

1 1. A ball-limiting metallurgy (BLM) stack comprising:
2 a metal adhesion first layer disposed above and on a metallization;
3 a metal second layer disposed above and on the metal adhesion first layer;
4 a metal third layer disposed above and on the metal second layer;
5 an electrically conductive bump disposed above and on the metal third layer;
6 and
7 wherein at least one of the metal second layer and the metal third layer
8 comprises copper.

1 2. The BLM stack according to claim 1, wherein the metal adhesion
2 first layer is selected from Ti, TiW, W, and Cr.

1 3. The BLM stack according to claim 1, wherein the metal second
2 layer comprises copper and the metal third layer is selected from a refractory metal,
3 a metal-doped refractory metal, or a refractory metal alloy.

1 4. The BLM stack according to claim 1, wherein the metal second
2 layer comprises copper and the metal third layer is selected from a refractory metal,
3 a metal-doped refractory metal, or a refractory metal alloy selected from Ni, Co, Pd,
4 Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-
5 solution or stoichiometric ratio.

1 5. The BLM stack according to claim 1, wherein the metal second
2 layer comprises copper and the metal third layer is selected from a nitrided
3 refractory metal, a nitrided metal-doped refractory metal, or a nitrided refractory
4 metal alloy selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo,
5 W, Sc, Y, La, and Ce in a solid-solution or stoichiometric ratio.

1 6. The BLM stack according to claim 1, wherein the metal third layer
2 comprises copper, and wherein the metal second layer is selected from a refractory
3 metal, a metal-doped refractory metal, or a refractory metal alloy.

1 7. The BLM stack according to claim 1, wherein the metal third layer
2 comprises copper and the metal second layer is selected from a refractory metal, a
3 metal-doped refractory metal, or a refractory metal alloy selected from Ni, Co, Pd,
4 Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y, La, and Ce in a solid-
5 solution or stoichiometric ratio.

1 8. The BLM stack according to claim 1, wherein the metal third layer
2 comprises copper and the metal second layer is selected from a nitrided refractory
3 metal, a nitrided metal-doped refractory metal, or a nitrided refractory metal alloy
4 selected from Ni, Co, Pd, Pt, NiV, CoV, PdV, PtV, Ti, Zr, Hf, Cr, Mo, W, Sc, Y,
5 La, and Ce in a solid-solution or stoichiometric ratio.

1 9. The BLM stack according to claim 1, wherein the metal second layer
2 comprises a copper layer and wherein the metal third layer comprises a copper stud

1 10. The BLM stack according to claim 1, further comprising:
2 an intermetallic layer disposed between the metallization and the electrically
3 conductive bump.

1 11. The BLM stack according to claim 1, wherein the electrically
2 conductive bump comprises a tin-lead solder composition selected from Sn37Pb,
3 Sn97Pb, and Sn_xPb_y , wherein $x+y$ total 1 and wherein x is in a range from about 0.3
4 to about 0.99.

1 12. A process comprising:
2 forming a metallization over a substrate;

3 forming a metal adhesion first layer above and on the metallization;
4 forming a metal second layer above and on the metal adhesion first layer;
5 forming a metal third layer above and on the metal second layer;
6 forming a solder bump above and on the metal third layer, and
7 wherein at least one of the metal second layer and the metal third layer
8 comprises sputtered copper.

1 13. The process according to claim 12, forming a metal adhesion first
2 layer further comprising:
3 sputtering a composition over the metallization under conditions to impart a
4 compressive stress in the metal adhesion first layer, wherein the composition is
5 selected from Ti, TiW, W, and Cr.

1 14. The process according to claim 12, forming the metal second layer
2 and forming the metal third layer further comprising:
3 sputtering a copper metal second layer over the metal adhesion first layer
4 under conditions to impart a compressive stress therein; and
5 sputtering the metal third layer under conditions to impart a compressive
6 stress therein, wherein the metal third layer is selected from a refractory metal, a
7 metal-doped refractory metal, or a refractory metal alloy.

1 15. The process according to claim 12, forming the metal second layer
2 and forming the metal third layer further comprising:
3 sputtering the metal second layer over the metal adhesion first layer and
4 under conditions to impart a compressive stress therein, wherein the metal third
5 layer is selected from a refractory metal, a metal-doped refractory metal, or a
6 refractory metal alloy; and
7 sputtering a copper metal third layer over the metal second layer under
8 conditions to impart a compressive stress therein.

1 16. The process according to claim 12, forming the metal second layer
2 and forming the metal third layer further comprising:
3 sputtering a copper metal second layer over the metal adhesion first layer
4 under conditions to impart a compressive stress therein; and
5 plating a copper stud through a mask that is disposed over the metal second
6 layer.

1 17. The process according to claim 12, further comprising:
2 forming an electrically conductive bump above and on the metal third layer.

1 18. A process comprising:
2 forming a copper pad over a metal-six (M6) metallization;
3 sputtering a Ti metal adhesion first layer above and on the metallization;
4 sputtering a metal second layer above and on the Ti metal adhesion first
5 layer;
6 forming a metal third layer above and on the metal second layer;
7 forming a solder bump above and on the metal third layer, and
8 wherein at least one of the metal second layer and the metal third layer
9 comprises copper.

1 19. The process according to claim 18, wherein sputtering a Ti metal
2 adhesion first layer above and on the metallization comprises:
3 sputtering a Ti composition over the metallization, wherein the Ti
4 composition has a thickness in a range from about 500 Å to about 4,000 Å.

1 20. The process according to claim 18, wherein sputtering a metal
2 second layer and forming a metal third layer comprise:
3 sputtering a NiV composition over the Ti metal adhesion first layer, wherein
4 the NiV composition has a thickness in a range from about 1,000 Å to about 5,000
5 Å; and

6 sputtering a Cu composition over the metal second layer, wherein the metal
7 third layer has a thickness in a range from about 1,000 Å to about 5,000 Å.

1 21. The process according to claim 18, wherein forming a metal third
2 layer comprises:
3 sputtering a NiV composition over the metal second layer, wherein the NiV
4 composition has a thickness in a range from about 1,000 Å to about 5,000 Å, and
5 wherein the metal second layer has a thickness in a range from about 1,000 Å to
6 about 5,000 Å.

1 22. The process according to claim 18, wherein forming a metal third
2 layer comprises:
3 electroplating a copper stud over the metal second layer, wherein the copper
4 stud has a thickness in a range from about 5 micrometers to about 15 micrometers,
5 and wherein the metal second layer has a thickness in a range from about 1,000 Å to
6 about 5,000 Å.

1 23. A system comprising:
2 a substrate comprising an electrical device;
3 a metallization pad disposed over the substrate;
4 a ball-limiting metallurgy disposed over the metallization pad, the ball-
5 limiting metallurgy comprising:
6 a metal adhesion first layer disposed above and on the metallization pad;
7 a metal second layer disposed above and on the metal adhesion first layer;
8 a metal third layer disposed above and on the metal second layer;
9 an electrically conductive bump disposed above and on the metal third layer;
10 wherein at least one of the metal second layer and the metal third layer
11 comprises copper; and
12 a flip-chip disposed over the ball-limiting metallurgy.

1 24. The system according to claim 23, wherein the flip-chip comprises a
2 solder having a composition of about Sn37Pb, and wherein the electrically
3 conductive bump comprises a solder having a composition of about Sn97Pb.

1 25. The system according to claim 23, wherein the electrical device
2 comprises a chip-scale package.

1 26. The system according to claim 23, wherein the flip-chip comprises a
2 chip-scale package.

1 27. The system according to claim 23, wherein the electrical device
2 comprises a chip-scale package and wherein the flip-chip comprises a chip-scale
3 package.

1 28. The system according to claim 23, further comprising:
2 an intermetallic zone that substantially isolates the metal third layer from the
3 electrically conductive bump.